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10/10/02

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,877	08/20/2001	Kiichi Yamashita	XA-9535	4057

7590 12/26/2002

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[REDACTED] EXAMINER

NGUYEN, KHAI M

[REDACTED] ART UNIT [REDACTED] PAPER NUMBER

2819

DATE MAILED: 12/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/931,877	YAMASHITA ET AL.
	Examiner Khai M. Nguyen	Art Unit 2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 20 August 2001.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-16 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3,4,5</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. However, Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

Abstract Objections

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Correction is required.

Drawings

3. Figures 3A-3B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Prentice (US 5,357,089).

Regarding claim 1, Prentice reference discloses a power amplifier module (Fig. 3) using a transistor (Q1) as an amplifying element, wherein the module includes an overcurrent detection circuit (sensor 30) for detecting the base current of the amplifying element (column 2, lines 55-58) above a predetermined value (or a previously set value), and subtracting the overcurrent from the base of the amplifying element (by reducing the impedance of the controllable resistance element 32 and by that the voltage or current at the base of the transistor is kept at a constant) and therefore the collector current in the transistor Q1 is also kept at a substantially constant value (lines 44-68 of column 2 to lines 1-10 of column 3).

Regarding claims 2-3, Prentice reference teaches a power amplifier module comprising: a bipolar transistor (Q1; column 3, lines 50-55) for receiving an input signal and generating an amplified signal; a bias circuit (the circuit portion that connected to the base of the transistor); and a protection circuit (30) for detecting the base current of the amplifying element (column 2, lines 55-58) above a predetermined value (or a previously set value), and subtracting the overcurrent from the base of the amplifying element (by reducing the impedance of the controllable resistance element 32 and by that the voltage or current at the base of the transistor is kept at a constant)

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and therefore the collector current in the transistor Q1 is also kept at a substantially constant value (an increase in the collector current is restricted) (lines 44-68 of column 2 to lines 1-10 of column 3).

Regarding claims 10-11, the Prentice reference (and/or the prior art Fig. 3A of the instant application) discloses that the amplifying element is a GaAs-HBT transistor or it can be any available transistor and constructed as in integrated circuit (column 3, lines 50-54).

Regarding claims 15-16, the above references discloses/teaches the amplifier module of the claimed invention except for the input signal is a voice signal and modulated, amplified, and transmitted to the external antenna; and a frequency synthesizer, modulator, demodulator and a voice-processing portion. It has been held that

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 4-9 and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prentice (US 5,357,089) in view of Sowlati et al. (US 6,300,837), Chiozzi (US 5,917,382), Maruyama et al. (US 6,329,879), and the applicants' admitted prior art (AAPA, Fig. 3A).

Regarding claims 4-5, Prentice reference discloses the amplifier module of the claimed invention except for the input and output matching circuits, and the bias circuit wherein it includes a current source and a transistor and the transistor constitutes a current mirror circuit along with other transistor connected in series with the current source. Sowlati et al. reference discloses an amplifier module having input/output matching circuits (118 & 104 respectively) and the bias circuit (120) including a current source (where it is controlled by a voltage source 140); a second transistor (124) being connected serially to the current source; and a current mirror circuit (123). It would have been obvious to one person having ordinary skill in the art at the time the invention was made to implement the bias circuit of Prentice reference by a substituting or replacing by another bias circuit such as the bias circuit as disclosing in the amplifier module of the Sowlati et al. reference because it is intended for biasing a current to the base of the bipolar transistor amplifier and at the same time that matching circuits can be provided for matching input and output impedances of the amplifier module.

Regarding claims 6 & 9, Prentice reference discloses the amplifier module of the claimed invention except for the particular structure of the protecting circuit. However, it is taught by the reference that the detecting circuit (30) can be implemented in many forms as seen in Figs. 9 &10 of the reference. The protecting circuit comprises parallel transistors, resistors, current mirrors, and diodes. It would have been obvious to one person having ordinary skill in the art at the time the invention was made to modify the protecting circuit, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japkse, 86 USPQ 70.

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Regarding claims 7-8, Prentice reference teaches the predetermined value of the base current of the amplifier module is made variable in accordance with a change in a power supply voltage (this voltage is the voltage that generated by the detecting circuit 30) except for the amplifier module does not explicitly show that it comprises an voltage to current converter; a power supply detecting circuit; and a current control circuit being coupled together. The AAPA (Fig. 3A) discloses a final stage of an amplifier module comprising a voltage to current converter, a power supply voltage detecting circuit (11), and a current control circuit (9). It would have been obvious to one person having ordinary skill in the art at the time the invention was made to incorporate these references in making a high frequency amplifier because with the protecting circuit (30) in the final stage of the amplifier module it protects the circuit being overloaded or shorts for example.

Regarding claims 12-14, it was taught that (by the Masashi et al., the reference provided by the applicants) in a high frequency power amplifier, a plurality of transistor amplifying stages are being coupled together (in order to have a sufficient gain) to form an amplifier module and the last stage of an amplifier module is provided with overcurrent/overvoltage protecting circuit (see Chiozzi reference US 5,917,382; column 1, lines 14-19) for protecting the module from shorts, for example. It would have been obvious to one person having ordinary skill in the art at the time the invention was made to incorporate these references by providing a high frequency power amplifier with the

protection circuit as taught by Prentice in order to prevent or protect the output amplifier from being overload or shorts.

Regarding claims 15-16, Prentice discloses the amplifier of claim 2 except for it is being used with a wireless communication system. Maruyama et al. teaches a wireless communication system, the system comprising: a high frequency amplifier (53), an antenna (57), a receiver (51), a frequency synthesizer (64), a voice processing portion (62), a modulator (66), and a demodulator (68), wherein a voice signal (from the microphone 57), and amplified by a power amplifier and transmitted to a antenna (55). It would have been obvious to one person having ordinary skill in the art at the time the invention was made to substitute the amplifier module as taught by Prentice with the high frequency amplifier 53 because this amplifier module has a overcurrent protection, it protects the wireless system from shorts or overloaded.

Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclose.

Prentice (US 5,357,089), Sowlati et al. (US 6,300,837), Sager (US 5,404,114), King (US 6,137,366), Wheatley, Jr. (US 3,786,364), Chiozzi (US 5,917,382), Naxera (US 4,789,842), Wheatley, Jr. (US 3,967,207), Kaplan (US 4,355,341), Maruyama et al. (US 6,329,879), and Metro et al. (US 5,343,141) disclose relevant art to the claimed invention.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 703-605-4244. The examiner can normally be reached on 8:30 to 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703- 308-7724 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-6789.

KN
December 23, 2002


Michael J. Tokar
Supervisory Patent Examiner
Technology Center 2800